JPEG IP

The JPEG IP (Intellectual Property) cores are intended for high-speed encoding and decoding of images according to ISO/IEC 10918-1 baseline coding standard.

The IP cores can be used with both ASIC and FPGA families. As our JPEG cores are very compact it will also fit in smallest FPGA devices.

The JPEG encoding/decoding does not require external DDR memory. For this reason, it is the ideal IP core for many applications with a good compromise between the quality, latency, complexity and compression ratio.

The encoding quality is fully configurable during run-time, including custom entropy and quantization tables.

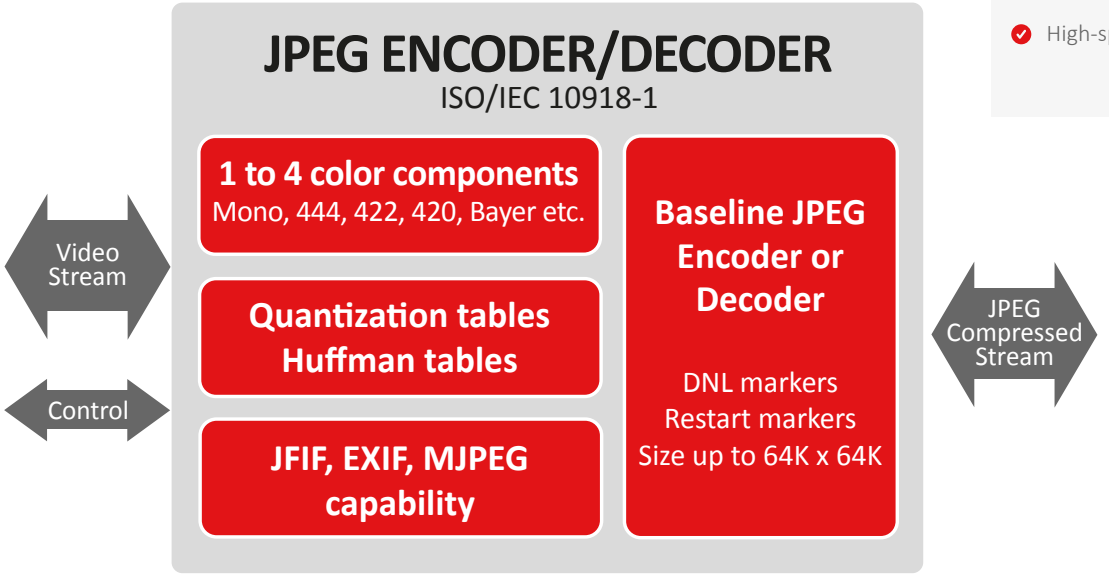
The simple FIFO-like interfaces and 100% synchronous structure of our JPEG IP cores make the integration very easy. The encoding and decoding of the image or video is handled autonomously by the IP core, without any CPU intervention.

Features

- ASIC and FPGA
- Compliant with baseline JPEG (ISO/IEC 10918-1)
- Unrestricted image resolutions up to 64K by 64K
- Chroma subsampling (4:4:4, 4:2:2, 4:2:0), grayscale and bayer support.
- Full header building and parsing capability:
  - User-definable comments
  - Application markers
  - Quantization tables
  - Huffman tables
- Support for full-format and abbreviated-format, including restart markers and restart interval

Applications

- Industrial imaging
- High-speed camera
- Data center
- Multi-media conferencing
- ...



Silex Insight
Rue Emile Francqui 11,
1435 Mont-Saint-Guibert, Belgium

Tel: +32 10 45 49 04
E-mail: contact@silexinsight.com
Web: www.silexinsight.com