SILEX INSIGHT

Product sheet
BA119

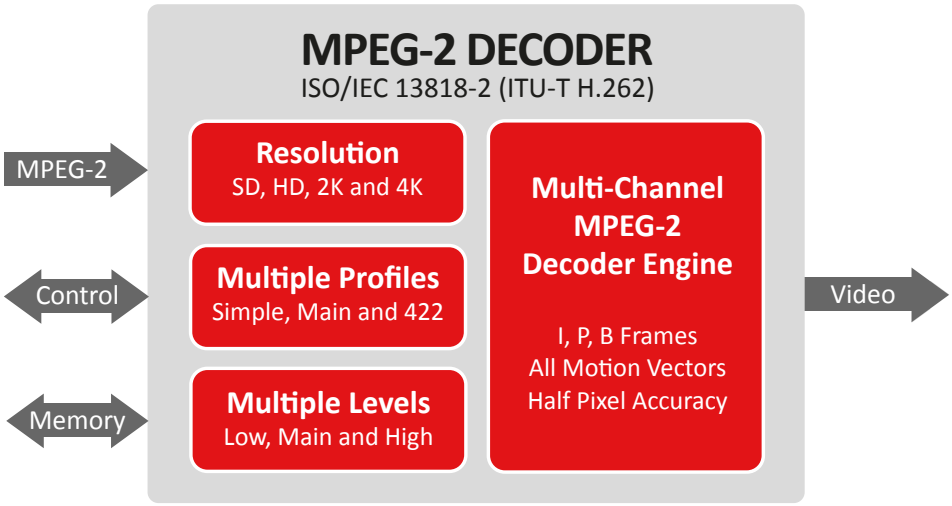
MPEG-2 DECODER IP

Our Mpeg2 decoder IP core can more than meet the requirements of demanding applications such as broadcast, production, digital cinema, video conferencing...

This flexible IP cores have already been proven in high-end market environments. It deliver real-time decoding of high-resolution and multi-channel video streams such as 2K, 4K, SD, HD...

The architecture provides the highest standards of:

- **Portability:** Support for all leading-edge FPGAs
- **Flexibility:** Easy to integrate interface
- **Performance:** Faster than real-time to support more simultaneous channels, larger images or higher frame-rate
- **Compactness:** Cost-effective, low resource count
- **Interoperability:** Compliant with MPEG-2 TS



Features

- ASIC and FPGA
- Compliant with ISO/IEC 13818-2 standard (ITU-T H.262)
- Simple, main and 422 profiles
- Low, main and high levels
- Multiple channels
- Intra and inter frame (I, P and B frames)
- SD, HD, 2K, 4K resolution
- Frame rate up to 120 fps for progressive full HD
- Interlaced and progressive format
- 4:2:2 and 4:2:0 Chroma formats
- 8 bits per pixel component
- 100% CPU offload

Applications

- Broadcast
- Production
- Digital cinema
- Video conferencing
- ...

Deliverables

- Netlist or RTL
- Simulation testbench
- Implementation example
- Bit accurate C model

V1.1

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