The video IP cores developed by Silex Insight using CFA (Bayer, Quad-Bayer) produces visually lossless video quality. The algorithm adds minimal latency to the system while it offers super-resolution.
Did you know?
Invented in 1976 by Bryce Bayer, the Bayer filter is perhaps the most well-known color filter arrays currently in use. Elegant in its simplicity, the well-known filter uses an array of RGB filters placed on a sensor array to allow image sensors to create color images. By using twice as many green as red or blue filter elements, the filter array was designed to more accurately emulate the physiology of the human eye since the eye is more sensitive to green wavelengths.

Substantial Reduction In File Size
- Storing the RAW Bayer data results in a substantial reduction in file data compared to the full raster RGB/YUV equivalent (uncompressed)

Increased Image Quality
- RAW Bayer data can be re-interpolated at a later stage as demosaic algorithms and methods improve, resulting in increased image quality.

High Performance With Low Power Computing
- In-house development of own video codec IP (JPEG 2000, VC-2 HQ)

Super Resolution
- Our IP cores can support any resolution
- Already delivered 24K encoding

Low Latency
- Reduce the bandwidth during real-time transmission over network infrastructures without affecting the latency.

Demosaising in FPGA/ASIC or Software
- Create viewable images from the raw data doing the demosaising (also known as Debayering) in the FPGA/ASIC or in software, depending on the use case.

APPLICATIONS
The digital camera system is typically formed by a lens system, an image sensor and an image processing pipeline. When an image is captured, the scene is first illuminated by the camera flash or by ambient lighting. The light beams then travel through a lens system and reach an image sensor. The image sensor creates a digital representation of the captured light. Raw image data is read from the sensor and transferred into the image processing (demosaicing) pipeline. The demosaicing can take place within the FPGA/ASIC or done by software.

**Benefits of Demosaicing in the FPGA/ASIC**

For real time applications where the compressed video is sent on the network, an implementation of a demosaicing algorithm on FPGA/ASIC is ideal thanks to the parallel processing nature of FPGA/ASICs.

Demosaicing in the FPGA/ASIC is ideal for handling live streams.

**Benefits of Demosaicing in Software**

For non-real time applications, performing the demosaicing in software can help get the best reduction in interpolation artifacts. For state of the art demosaicing algorithms that are difficult to implement in hardware because of their memory requirement and complex access patterns

Demosaicing in the software is ideal when memory and computational requirements are very high.
WHEN YOUR DATA NEEDS TO BE RAW!

VIDEO CODEC

<table>
<thead>
<tr>
<th>Features</th>
<th>JPEG 2000</th>
<th>VC-2 HQ</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FLEXIBLE AND ROBUST</td>
<td>SUPERIOR LIGHTWEIGHT</td>
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<td></td>
<td>HIGH QUALITY VIDEO CODEC</td>
<td>SLICE-BASED VIDEO CODEC</td>
</tr>
<tr>
<td></td>
<td>EMMY® Award-winning IP-CORES SOLUTIONS!</td>
<td>Incredible low latency 0.0593 milliseconds!</td>
</tr>
</tbody>
</table>

Our IP cores can encode or decode JPEG 2000 images and video with unrivalled quality, high-speed and compact footprint. The encoding and decoding are compliant with the ISO/IEC 15444-1 specification. It has been successfully integrated by market leaders in digital cinema, broadcast, defense, storage and video surveillance applications.

The high quality profile and low delay syntax of VC-2 is used to achieve low compression ratio, typically up to 4 times visually lossless. The algorithm is lightweight and works without external memory allowing cost-effective implementation. The VC-2 High Quality codec has ultra-low latency due to its slice-based processing.

**Image**

<table>
<thead>
<tr>
<th>Color format</th>
<th>RAW (CFA-BAYER and others)</th>
<th>VC-2 HQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit depth</td>
<td>8 / 10 / 12 / 14 / 16 bits</td>
<td>Any</td>
</tr>
<tr>
<td>Resolution</td>
<td>Any</td>
<td>Any</td>
</tr>
<tr>
<td>Frame rates</td>
<td>Any</td>
<td>Any</td>
</tr>
<tr>
<td>Compression Ratio</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

**Processing**

<table>
<thead>
<tr>
<th>Quality</th>
<th>Visually lossless down to 1bpp</th>
<th>Visually lossless down to 2bpp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rate control</td>
<td>Constant bit rate or capped variable bit rate</td>
<td></td>
</tr>
<tr>
<td>Latency</td>
<td>&lt; 1 frame</td>
<td>Down to 0.0592 milliseconds</td>
</tr>
</tbody>
</table>

**Platform**

| Easy implementation | FPGA / ASIC | FPGA / ASIC (No DDR) |

For additional information, please contact your local sales representative or visit our website [www.silexinsight.com](http://www.silexinsight.com)

We can also deliver standard RGB/YUV video codec (JPEG 2000 / VC-2 HQ) if needed.

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Global sales offices
Worldwide customer base
Founded in 1991

Silex Insight = Silicon experts with know-how
Expertise on PCB design, FPGA and ASIC
Design Services to fully develop to your needs

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